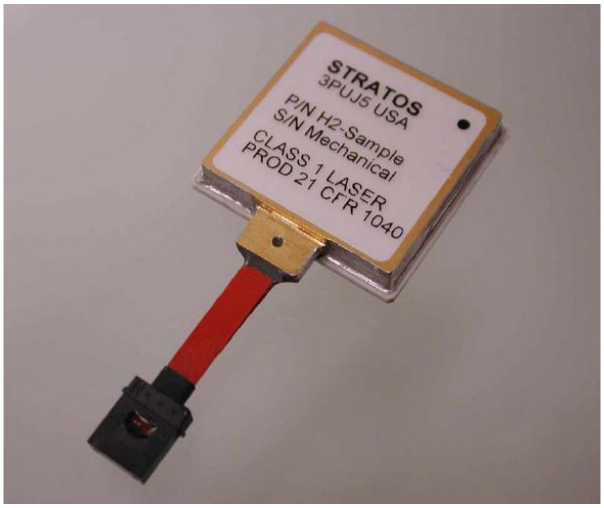
Stratos
H2-TR4-Sxxx
Hybrid Technology Quad Optical Transceiver

Connectivity for Business Critical Continuity

Four Ports, 2.125 Gbps, 3.3V, 850nm VCSEL, Multimode, Up to 700M Link Distance



Key Features & Benefits

- Four independent TX and RX ports at 2.125 Gbps each
- Small footprint 1.00 inch square
- Low height, less than 0.285 inches max
- Fiber Flex with custom lengths and termini
- BGA socket surface mount, no through holes required
- Removable device (from BGA socket) for IR reflow
- Industrial temp range, vibration tolerant design
- SPI control interface for software control and status
- Control for RX Data Squelch on Loss of Signal
- Control for TX optical Enable/Disable
- Status for RX Signal Detect and Signal Strength
- 3.3V Power, 1.6W max

Ordering Information

H2	-	TR4	-	Sxxx

The –Sxxx suffix represents unique part numbering for fiber route and termini options. See page 22 or consult the factory for details and for custom part numbering for your application.

Applications

The H2-TR4-Sxxx Quad Port Hybrid Transceiver provides a highly ruggedized, small footprint, cost effective solution for 1 to 2.5Gbps multimode optical data links. The device includes an integrated Fiber Flex cable terminated into an industry standard 1x12 MT connector. The device may be customized to have different Fiber Flex lengths, custom fiber flex routing, or use alternate types of fiber termini such as ST, SC, or MIL-T-29504. A complete list is provided in the Ordering Options section of this data sheet. These transceivers are designed to operate for 1x/2x Fiber Channel Links, but can be used for any other data communications purpose within their operating parameters, up to 2.5 Gbps per port.

Product Overview

The **Emerson Network Power Connectivity Solutions** H2-TR4-Sxxx Quad Port Hybrid Transceiver consists of a VCSEL and PIN Diode Array, Laser Driver, Post Amp circuits, a microcontroller, and integrated fiber flex with MT termination. The electrical signals are routed through a BGA surface mount pin/socket connector to allow easy removal of the entire assembly and to support BGA reflow thermal profiles for ease of PCB assembly. The transmitter accepts four sets of differential data and drives a quad 850nm VCSEL array. The VCSEL drive circuit includes a temperature sensor circuit to drive temperature compensation of the optical output level in order to maintain stable output power level over the thermal range. The internal microprocessor provides software control for each individual transmit port for TX Enable/Disable and TX diagnostics. The receiver uses a quad 850nm GaAs PIN array, post amplifier, and outputs four sets of differential data. The internal microprocessor enables software control or read for individual port RX Signal Detect, RX Squelch enable/disable, and Receive Signal Strength Indicators (RSSI). The data interface for the device is a 100Ω differential pair, 50Ω impedance per line, and is CML compliant. Individual LVTTL hardware status pins are provided for RX Signal Detect, RX Enable, TX Enable, and TX Fault. The hardware control allows an FPGA or other hardware device to control and monitor the main functions of the Hybrid Transceiver. Software control is provided using a Serial Peripheral Interface (SPI) 4-wire bus. The SPI bus operates in a bit-serial fashion at clock rates up to 2MHz. The internal registers are addressed through a 3 byte read or write sequence. The control and status of the device via software is not required for operation, and is provided purely as an enhancement to operation. The Power Up default SPI register values are all configured for normal operation on all channels, thereby allowing the transceiver's control pins to configure the device without any SPI activity.

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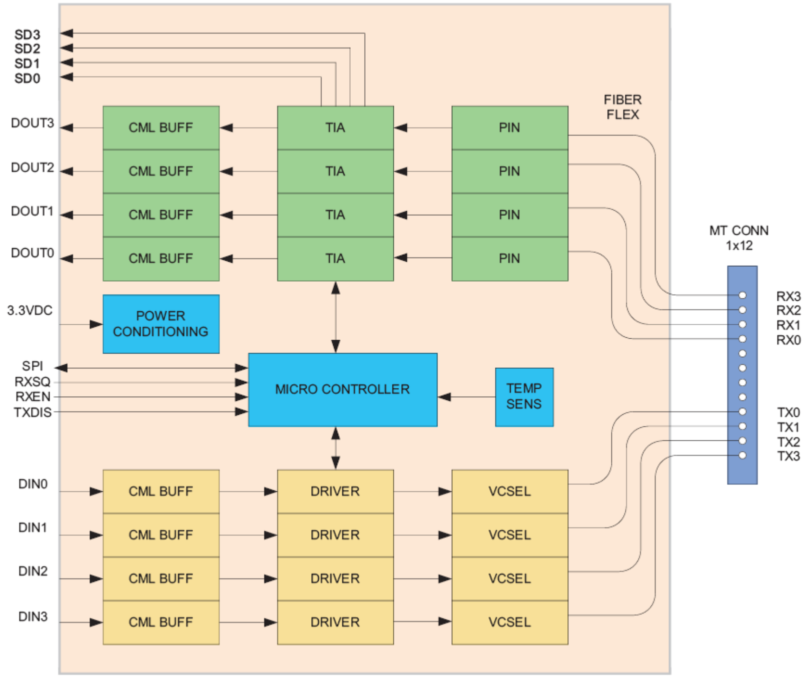
Block Diagram



BGA Socket Operation

The H2-TR4-Sxxx Quad Port Hybrid Transceiver uses a surface mount micro BGA socket, which is constructed of high temp G-11 material and houses an array of socket contacts. The BGA socket is soldered to the application card through normal IR or Thermal oven reflow cycles. There are not any through-hole pins, allowing the device to be used in solid core-board type applications. The actual transceiver device, which contains the active circuits, optics, and Fiber Flex pigtail, has an array of pins located on the bottom of the device that insert into the surface mount BGA socket. The transceiver is inserted into the BGA socket with approximately 15 pounds of force. The entire structure consisting of the BGA socket and the transceiver device fits within 0.285 inch maximum height. The transceiver is removed by using a pull tool to lift the transceiver pins from the BGA socket. The entire structure is designed to withstand avionics vibration and shock requirements, yet allow ease of manufacturing and re-work.

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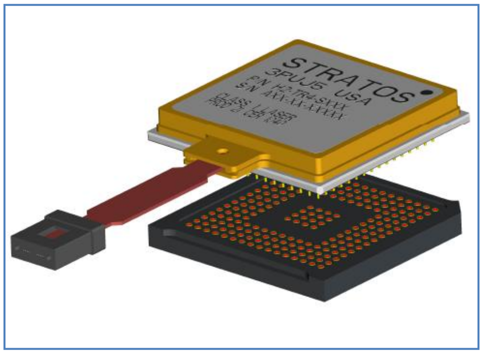

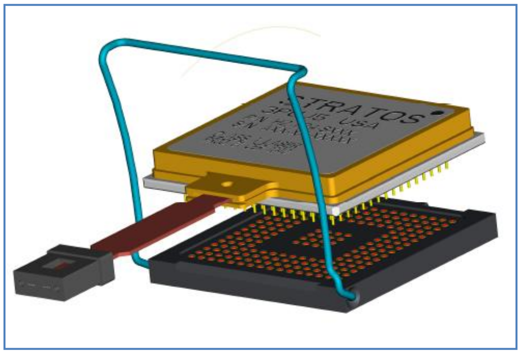

Absolute Maximum Ratings

Absolute maximum limits mean that no catastrophic damage will occur if the product is subjected to these ratings for short periods, provided each limiting parameter is in isolation and all other parameters have values within the performance specification. It should not be assumed that limiting values of more than one parameter can be applied to the product at the same time.

Parameter	Symbol	MIN	Typical	MAX	Unit
Storage Temperature	T_S	-55		+125	°C
BGA Socket Soldering Temperature	T_{SOLD}			+270	°C
Lead Soldering Time	t_{SOLD}			10	Seconds
Supply Voltage	V_{CC}	-0.5		+3.6	V
Data Input Voltage	V_I	-0.5		V_{CC}	V
Differential Input Voltage (p-p)	V_D			2.2	V

Recommended Operating Conditions

Parameter	Symbol	MIN	Typical	MAX	Unit
Operating Temperature Limit – Case	T_C	-40		+85	°C
Storage Temperature – Long Term	T_S	-40		+100	°C
Supply Voltage	V_{CC}	+3.135		+3.465	V
Differential Data Output Voltage Swing (p-p)	V_{DO}	300		800	mV
Differential Data Input Voltage Swing (p-p)	V_{DI}	200		800	mV
Differential Data Impedance	Z_I	80	100	120	Ω
Differential Data Impedance, Single Ended	R_L		50		Ω
Control Signal Input Voltage High	V_{IH}	2.2		V_{CC}	V
Control Signal Input Voltage Low	V_{IL}	V_{EE}		0.5	V
Status Signal Output Voltage High[1]	V_{OH}	2.4		V_{CC}	V
Status Signal Output Voltage Low[2]	V_{OL}	V_{EE}		0.4	V
Supply Current	I_{CC}	200		400	mA

1. Current Output High (Ioh) = -10.0mA max
2. Current Output Low (Iol) = 8.5mA max

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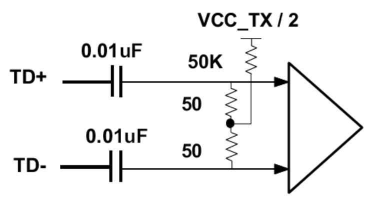
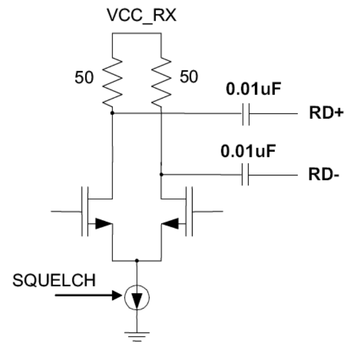
Detail of Data I/O Stages

AC Coupled CML Input Stage



AC Coupled CML RD+/- Output Stage



Transmitters: VCCTX = 3.135V to 3.465V, T_A = Operating Temperature Range

Parameter	Symbol	MIN	Typical	MAX	Unit
Optical Output[1]	P_O	-6.0	-3.0	-0.5	dBm
Optical Output Wavelength	λ_{OUT}	830	850	860	nm
Spectral Width	$\Delta\lambda_{RMS}$			0.85	nm
Extinction Ratio	ER	7	9		dB
Total Jitter (TX contribution, p-p)	Tj			114	psec
Deterministic Jitter (TX contribution, p-p)	Dj			56	psec
Relative Intensity Noise	RIN			-117	dB/Hz
Optical Modulation Amplitude (p-p)	OMA	196			μW

1. BER=10^{-12} @ 2.125 GigaBaud, PRBS = 2^7-1, NRZ

Receivers: VCCTX = 3.135V to 3.465V, T_A = Operating Temperature Range

Parameter	Symbol	MIN	Typical	MAX	Unit
Optical Sensitivity[1,2]	P_I	-16.0	-18.0		dBm
Receiver Saturation	P_{SAT}			0.0	dBm
Optical Wavelength	λ_{IN}	830		860	nm
Optical Modulation Amplitude[1,2]	OMA	36.5	25		μW
Signal Detect Assert Time	t_{SDAS}		<10	100	μS
Signal Detect Deassert Time	t_{SDDA}		<10	350	μS
Signal Detect Deassert Level[3]	SD_{OFF}	-26.5			dBm
Signal Detect Assert Level	SD_{ON}			-16.5	dBm
Signal Detect Hysteresis	HYS	1.0	2.0	3.0	dB
Total Jitter (RX contribution, p-p)	Tj			150	psec
Deterministic Jitter (RX contribution, p-p)	Dj			47	psec

1. BER=10^{-12} @ 2.125 GigaBaud, PRBS = 2^7-1, NRZ
2. Assuming an Extinction Ratio of 8dB or higher
3. RX data outputs are squelched when Signal Detect is deasserted to prevent noise data output when no optical signal is present

Link Distances

Fiber Specification	Application	Distance
50/125 (4700MHz*Km)	2X Fiber Channel (2.125Gbps)	700M

Fiber type: Corning OM4 50/125/245 Multimode Fiber

Regulatory Compliance

Requirement	Feature	Condition	Notes
MIL-STD-883-3015.7	ESD	Class II	2200V
IEC-801-2	ESD	Human Body Model	25KV
IEC-801-3	EMI	Immunity	10V/M
FCC	EMI	Class B	>20dB
EN 55022 (CISPR 22A)	EMI	Class B	10V/M
IEC-825 Issue 1993-11	Eye Safety	Class 1	TUV Certificate Number – In Process
FDA CDRH 21-CFR 1040	Eye Safety	Class 1	CDRH Accession Number – In Process

BGA Pin-Out, Application Card Footprint, Top View

Q	P	O	N	M	L	K	J	H	G	F	E	D	C	B	A	
GND	GND	GND	S CLK	S CSX	SIN	S OUT	NC	NC	GND	RX EN	NC	GND	NC	NC	GND	1
GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	NC	2
GND	GND	GND	VDD	VDD	VDD	GND	GND	GND	GND	VDD	VDD	VDD	VDD	GND	NC	3
NC	GND	VDD	VDD	VDD	VDD	GND	GND	GND	GND	VDD	VDD	VDD	VDD	GND	SQ EN	4
RST	GND	VDD	VDD									VDD	VDD	GND	RX SD3	5
TX EN	GND	VDD	VDD									VDD	VDD	GND	RX SD2	6
NC	GND	GND	GND			GND	GND	GND	GND			GND	GND	GND	RX SD1	7
RDY	GND	GND	GND			GND	GND	GND	GND			GND	GND	GND	RX SD0	8
FLT	GND	GND	GND			GND	GND	GND	GND			GND	GND	GND	NC	9
GND	GND	VDD	VDD			GND	GND	GND	GND			VDD	VDD	GND	GND	10
TD0 -	GND	VDD	VDD									VDD	VDD	GND	RD0 +	11
TD0 +	GND	VDD	VDD									VDD	VDD	GND	RD0 -	12
GND	GND	VDD	VDD	GND	GND	GND	GND	GND	GND	GND	GND	VDD	VDD	GND	GND	13
TD1 -	GND	VDD	VDD	GND	GND	GND	GND	GND	GND	GND	GND	VDD	VDD	GND	RD1 +	14
TD1 +	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	RD1 -	15
GND	TD2 -	TD2 +	GND	TD3 -	TD3 +	GND	GND	GND	GND	RD3 -	RD3 +	GND	RD2 -	RD2 +	GND	16

Pin Functions – Power and Ground

Pin Number	Symbol	Description	Logic Family
A1, D1, G1, O1, P1, Q1, Q2, Q3, A10, Q10, A13, Q13, A16, D16, G16, H16, J16, K16, N16, Q16, B2, C2, D2, E2, F2, G2, H2, J2, K2, L2, M2, N2, O2, P2, B3, G3, H3, J3, K3, O3, P3, B4, G4, H4, J4, K4, P4, B5, P5, B6, P6, B7, C7, D7, G7, H7, J7, K7, N7, O7, P7, B8, C8, D8, G8, H8, J8, K8, N8, O8, P8, B9, C9, D9, G9, H9, J9, K9, N9, O9, P9, B10, G10, H10, J10, K10, P10, B11, P11, B12, P12, B13, E13, F13, G13, H13, J13, K13, L13, M13, P13, B14, E14, F14, G14, H14, J14, K14, L14, M14, P14, B15, C15, D15, E15, F15, G15, H15, J15, K15, L15, M15, N15, O15, P15	GND	Power and Signal Return, 500mA max	GND
C3, D3 C12, D12, C13, D13, C14, D14, C4, D4, C5, D5, N12, O12, N13, O13, N14, O14, N3, N4, O4, N5, O5, E3, F3, E4, F4, C6, D6, C10, D10, C11, D11, L3, M3, L4, M4, N6, O6, N10, O10, N11, O11	VDD	3.3VDC Power, 200mA max	POWER

Pin Functions – Transmitter Data and H/W Control

Pin Number	Symbol	Direction	Description	Logic Family
Q12, Q11	TD0+, TD0-	I	Differential TX Data, Channel 0	CML
Q15, Q14	TD1+, TD1-	I	Differential TX Data, Channel 1	CML
O16, P16	TD2+, TD2-	I	Differential TX Data, Channel 2	CML
L16, M16	TD3+, TD3-	I	Differential TX Data, Channel 3	CML
Q6	TXEN[1]	I	TX Enable, All Channels (1=Enable, 0=Disable, 4.7KΩ internal pull-up)	LVTTL
Q9	FAULT[2]	O	TX Fault Status (1=Fault, 0=No Fault)	LVTTL
Q8	RDY[3]	O	Power Up Reset operation complete, Self Tests complete, Ready for Normal operation, rising edge of RDY will occur within 100msec of Power-up or rising edge RESET. (Rising Edge = Ready)	LVTTL

1. TXEN also requires the SPI register TXEN to be in the enable state before ENABLE condition is achieved
2. FAULT is set or cleared as a summary fault condition of the VCSEL. The individual channel faults are available via the SPI registers
3. RDY will assert 1 at RESET or powers up followed by deassert 0 approx. 55ms later. The subsequent rising edge of RDY indicates completion of the device initialization sequence.

Pin Functions – Receiver Data and H/W Control

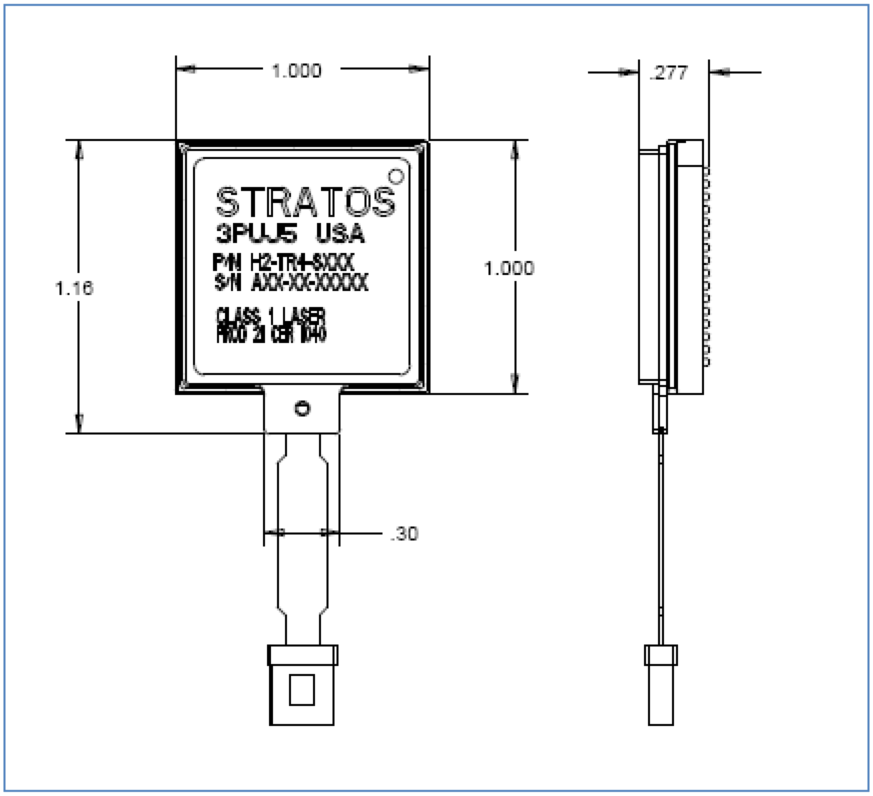
Pin Number	Symbol	Direction	Description	Logic Family
A11, A12	RD0+, RD0-	O	Differential RX Data, Channel 0	CML
A14, A15	RD1+, RD1-	O	Differential RX Data, Channel 1	CML
B16, C16	RD2+, RD2-	O	Differential RX Data, Channel 2	CML
E16, F16	RD3+, RD3-	O	Differential RX Data, Channel 3	CML
A8	RXSD0[1]	O	RX Signal Detect, Channel 0 (1=Input Optical Signal Detected, 0=No Signal)	LVTTL
A7	RXSD1[1]	O	RX Signal Detect, Channel 1 (1=Input Optical Signal Detected, 0=No Signal)	LVTTL
A6	RXSD2[1]	O	RX Signal Detect, Channel 2 (1=Input Optical Signal Detected, 0=No Signal)	LVTTL
A5	RXSD3[1]	O	RX Signal Detect, Channel 3 (1=Input Optical Signal Detected, 0=No Signal)	LVTTL
A4	SQEN	I	Squelch Enable, All Channels (1=Squelch Enable, 0=Disable, 4.7KΩ internal pull-up)	LVTTL
F1	RXEN[2]	I	RX Enable, All Channels (1=Enable, 0=Disable, 4.7KΩ internal pull-up)	LVTTL

1. The RXSDx status pins are valid only if the RXEN H/W pin and SPI resisters are in the ENABLE state (=1). If the receiver is in the DISABLE state, then the RXSDx lines are driven HI (=1).
2. RXEN also requires the SPI register RXEN to be in the enable state before ENABLE condition is achieved.

Pin Functions – S/W Control, Emulator, Test Points, N/C

Pin #	Symbol	Direction	Description	Logic
L1	SIN	I	SPI Port Data In	LVTTL
K1	SOUT	O	SPI Port Data Out	LVTTL
N1	SCLK	I	SPI Clock	LVTTL
M1	SCSX	I	SPI Port Chip Select (0=Select, 1=Not Selected, internal 4.7KΩ pull-up)	
Q5	RESET	I/O	Low True Reset with internal 4.7K pull-up. Also used for Emulator Clock. The minimum pulse low to activate RESET is 20usec.	LVTTL
Q7, E1, Q4, J1, H1, A2, A3, B1, C1, A9,	N/C	N/C	These pins allow this device to remain footprint complaint with the previous Hybrid Transceiver design HTP-TR4-S1xx. The pins are recommended for No Connect on new designs.	N/C

H2-TR4-Sxxx Shown with H2-TR4-SKT Socket (No Clip)



Hybrid Assembly
All dimensions ± .005 unless noted

BGA Socket Detail*

Parameter	Value
BGA Contact Plating	50 micron Gold over 100 micron Nickel
BGA Array Size	16x16, 1.27mm spacing
BGA Contact Size	0.036 inch diameter
Number of Contacts	208
Insertion Force (208 pins)	15 pounds initial, 7 pounds subsequent insertions
Extraction Force	7 pounds
Mating Durability	100 cycles minimum
Solderability	235 C for 2 seconds, do not exceed 270 C for 10 seconds

* See page 23 for mechanical detail.

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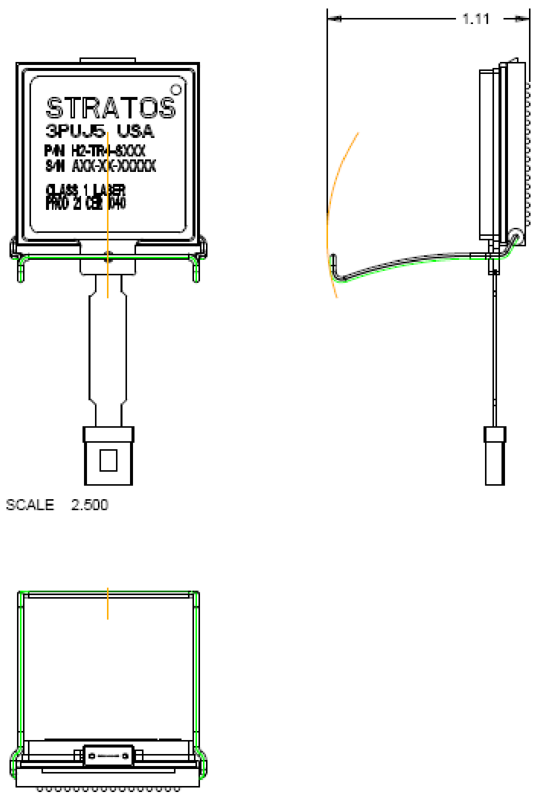
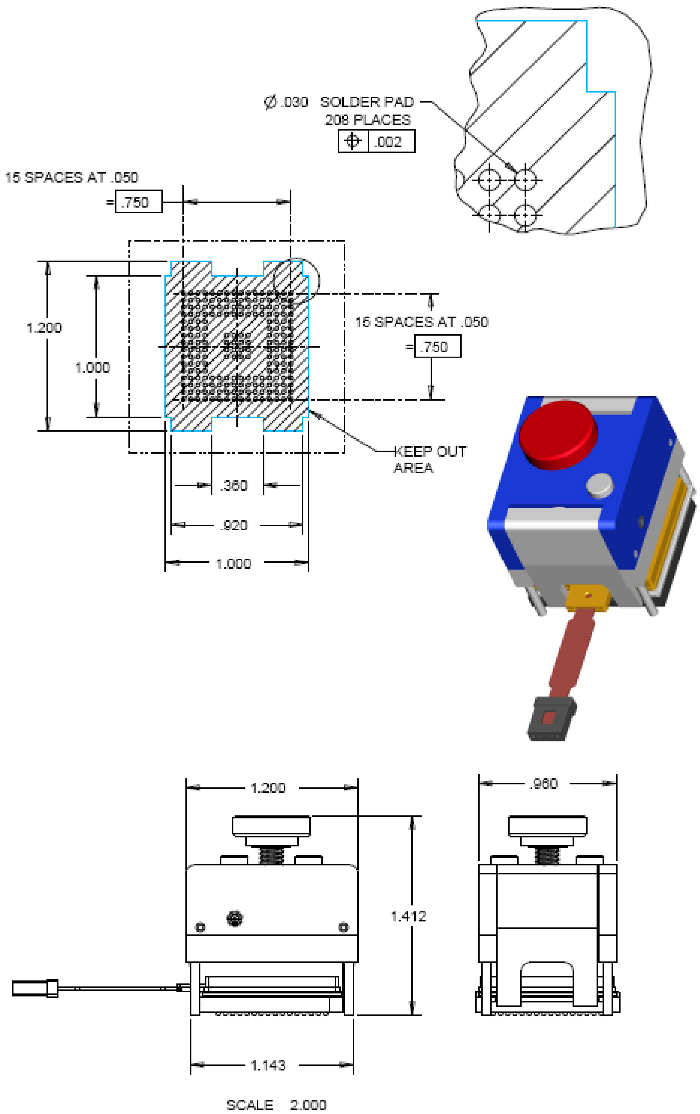
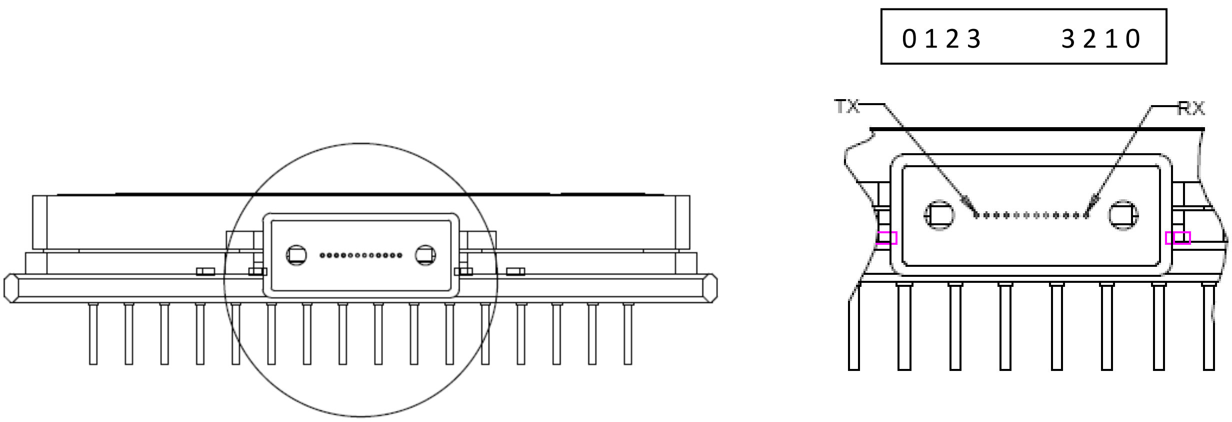


Hybrid Assembly with Socket and Clip



Extractor with Hybrid Assembly

Straight Route Detail of MT Fiber Connector

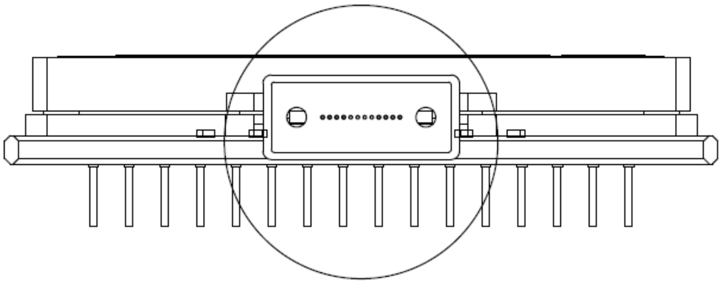


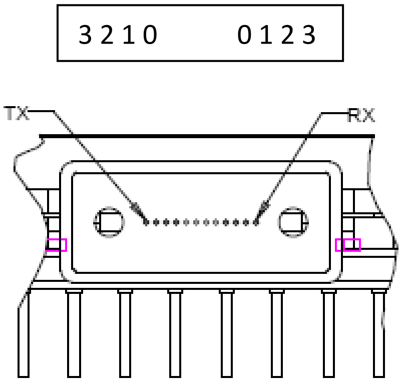
Straight Route MT12 Fiber Connector Optical Signal Description

Pin Number	Symbol	Direction	Description
F1	TX0	O	Optical TX Channel 0
F2	TX1	O	Optical TX Channel 1
F3	TX2	O	Optical TX Channel 2
F4	TX3	O	Optical TX Channel 3
F5	N/C		Reserved for Future
F6	N/C		Reserved for Future
F7	N/C		Reserved for Future
F8	N/C		Reserved for Future
F9	RX3	I	Optical RX Channel 3
F10	RX2	I	Optical RX Channel 2
F11	RX1	I	Optical RX Channel 1
F12	RX0	I	Optical RX Channel 0

Direction O = Output from the optical transceiver
Direction I = Input to the optical transceiver
MT12 Fiber is 50/125 micron multimode

Optional Shuffle Route Detail of MT Fiber Connector





Shuffle Route MT12 Fiber Connector Optical Signal Description

Pin Number	Symbol	Direction	Description
F1	TX3	O	Optical TX Channel 3
F2	TX2	O	Optical TX Channel 2
F3	TX1	O	Optical TX Channel 1
F4	TX0	O	Optical TX Channel 0
F5	N/C		Reserved for Future TX Channel 5
F6	N/C		Reserved for Future TX Channel 4
F7	N/C		Reserved for Future RX Channel 4
F8	N/C		Reserved for Future RX Channel 5
F9	RX0	I	Optical RX Channel 0
F10	RX1	I	Optical RX Channel 1
F11	RX2	I	Optical RX Channel 2
F12	RX3	I	Optical RX Channel 3

Direction O = Output from the optical transceiver
Direction I = Input to the optical transceiver
MT12 Fiber is 50/125 micron multimode

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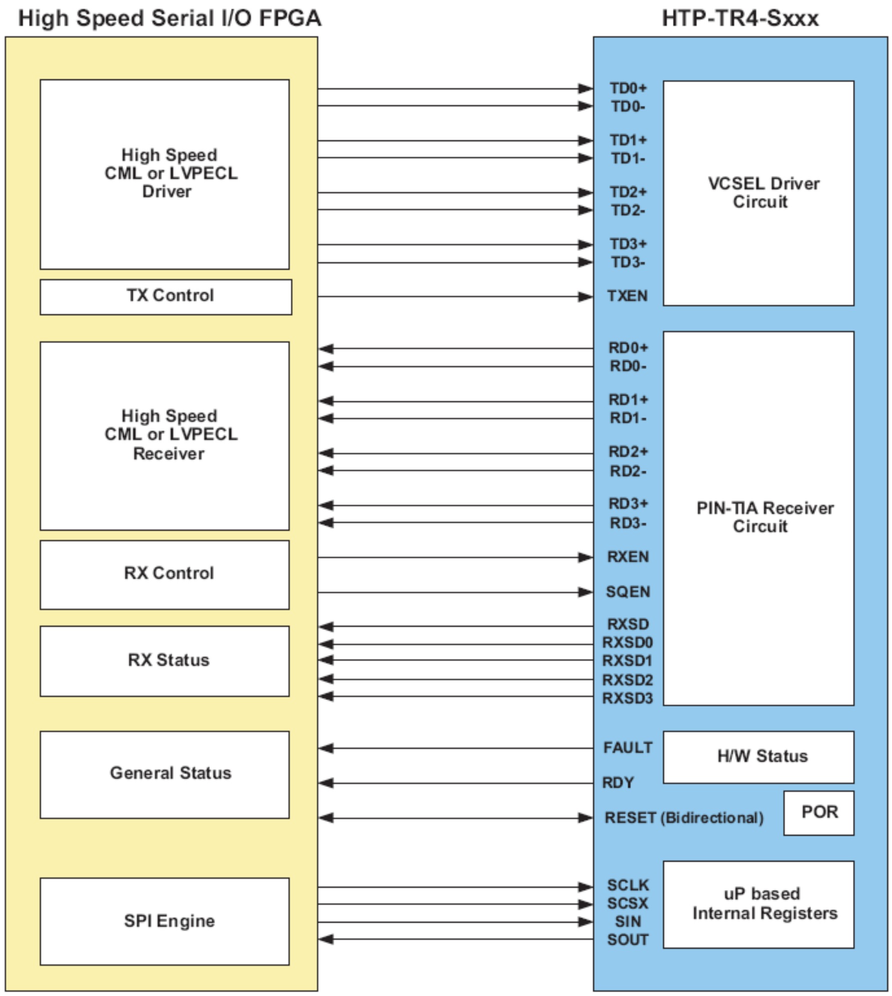
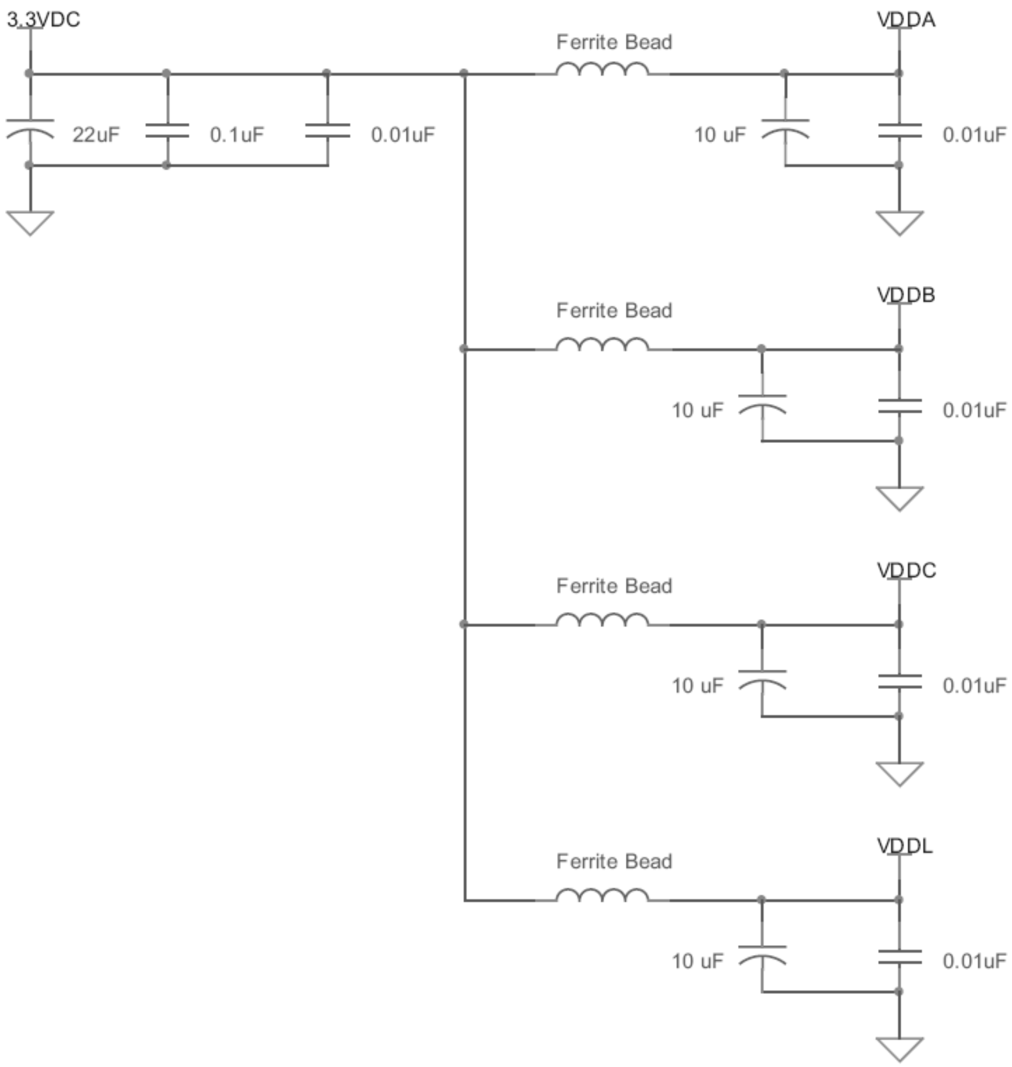
Application Block Diagram



Notes:

1. High speed TDX+/- and RDX+/- signals are CML compliant, AC coupled, and will work with either CML or LVPECL driver/receiver logic in the FPGA.
2. Keep high speed data signals routed using proper 50Ω impedance, 100Ω differential routes, taking care to keep both signals in the differential pair at same trace length.
3. The RESET signal is bidirectional, and may be driven by the Power On Reset (POR) circuit in response to a brown out condition detected on the internal Power Supply Monitor.
4. The SPI bus may be multiple slaves, with SCLK continuously running, and SCSX used to select those transactions for this particular device.

Recommended Power Supply Filtering



Notes:

1. Ferrite Bead recommendation MuRata BLM21A601S, provide 600Ω at 100MHz or better.
2. Place 10uF and 0.01uF capacitors as close as practical to the associated power pins on the device.

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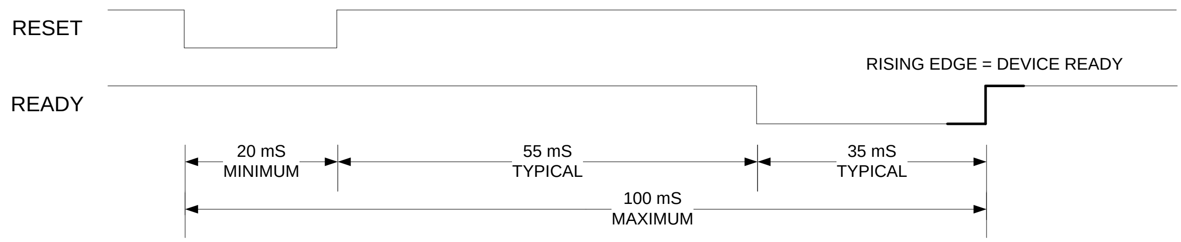
Power Up, Reset, Ready, and Fault Operation

The Hybrid Transceiver contains an internal Power Supply monitor circuit, which will hold the device in RESET until the power conditions are acceptable (about 2.7V). At this time, the Power On Reset circuit will release the RESET and allow the Hybrid Transceiver to initialize. The RESET is open collector, and the application card may continue to hold RESET low until some future time.

Once RESET is released by all sources, the Hybrid Transceiver will perform an internal self-test and then initialize for power-up default operation. The READY pin will be driven true (=1) following the rising edge of RESET. Approximately 55 mS later the READY pin will be driven low (=0) for approximately 35 mS. The subsequent *rising edge* of READY pin is the indication that the device is ready for data and SPI port communications. The maximum time from rising edge RESET to rising edge READY condition is 100msec.



After READY is issued, the Hybrid Transceiver will monitor the transceiver for TX VCSEL fault conditions. If any of the enabled TX channels have a VCSEL fault, the Hybrid Transceiver will issue a FAULT status for both the H/W pin and in the internal SPI register. Operation continues as normal. The H/W FAULT status is removed once the VCSEL fault condition clears. A latched version of the fault status is kept in the SPI register and is reset upon read.

Channel Enable/Disable, Squelch, and Signal Detect Operation

Once the Power up and Self Test operations are complete, the Hybrid Transceiver is ready for normal operation. The TX and RX channels are enabled or disabled through both H/W and SPI register settings. To enable the TX operation, the TXEN H/W pin must be controlled to the ENABLE state, and the internal SPI register TXEN must be configured for each enables channel. It is possible to enable/disable individual channels through the SPI register TXEN settings. When a TX channel is DISABLED, the associated circuitry is powered down within the Hybrid Transceiver within 10msec. Upon ENABLE control via the H/W pin or SPI register control, the associated TX channel will resume normal operation within 10msec.

To enable the RX operation, the RXEN H/W pin must be controlled to the ENABLE state, and the internal SPI register RXEN must be configured for each enabled channel. It is possible to enable/disable individual channels through the SPI register RXEN settings. When an RX channel is DISABLED, the associated circuitry is powered down within the Hybrid Transceiver within 10msec. Upon ENABLE control via the H/W pin or SPI register control, the associated RX channel will resume normal operation within 10msec. If the RX channel is DISABLED the RX Data output signals will be turned off (AC coupled, no transitions).

In many systems, it is desirable to squelch the RX data to a known state whenever the RX optical signal is lost, in order to prevent random noise data from propagating through the system. The Hybrid Transceiver may be configured to squelch the RX data on loss of signal by controlling the H/W SQEN pin. This function is under H/W control only; there is not a corresponding SPI register to control the SQEN state. If the Hybrid Transceiver is configured for SQEN, the RX Data output signals will be turned off (AC coupled, no transitions) if the optical signal is not detected. The SQEN control affects all RX channels; there is not an individual control for each RX channel.

The Hybrid Transceiver will monitor the RX optical signal and issue a Signal Detect status on each individual channel is a valid modulated optical signal is detected. The RXSD status is available through both H/W status pins and SPI registers. There is also a summary H/W Signal Detect RXSD pin representing the wire-OR of the individual RXSD0 through RXSD3 status. The RXSD and RXSD0 through RXSD3 H/W pin status are valid only if the receiver channel is ENABLED (via the H/W pin and SPI registers).

The Hybrid Transceiver will monitor the incoming TX Data activity on each individual channel. If data is detected on the incoming TX Data lines, the corresponding status bit will be set in the TXSD SPI register. There is not a corresponding H/W status pin for this function. The TXSD test circuit is after the TD+/- differential receiver, therefore the logic cannot be used to detect a fault on a single leg TD+ or TD- by itself. The application card may choose to test each individual leg in isolation and check for TXSD condition as a diagnostic test.

SPI Port Operation

The Hybrid Transceiver can be controlled through the SPI bus interface, in order to allow S/W configuration and control for several parameters. The Transceiver register map and theory of operation is presented in this section. Timing and SPI waveforms are presented in the following section.

The SPI interface is a 4 wire bus with Chip Select (SCSX), Serial Data In (SIN), Serial Data Out (SOUT), and Serial Clock (SCLK). The device operates in the slave mode, so the SCLK, SIN, and SCSX are always inputs (data to the Hybrid Transceiver), and SOUT is always a tri-stateable output (data from the Hybrid Transceiver). Data is transmitted and received Most Significant Bit (MSB) first.

SPI Op Code

The SPI operation is initiated by the SPI Master by driving SPI Chip Select low (SCSX = 0). All transfers are 3 bytes long. The first byte contains the Op Code (Most Significant 2 bits) and Register Address (Least Significant 6 bits). The MSB byte aligned Op Code value may be 0x40 (READ) or 0x00 (WRITE). All other op codes (0xc0 and 0x80) will result in no operation. Once the Op Code/Register Address byte is received, the Hybrid Transceiver will execute the READ operation or prepare for a WRITE operation. If the operation is READ, the Hybrid Transceiver will go read the specified register and prepare to return the value to the SPI Master. If the operation is a WRITE, the Hybrid Transceiver will accept the second byte as the new Data value for the specified register.

SPI WRITE Sequence

Command sequence (SIN): OP CODE/REG, WDATA, NULL.
Response sequence (SOUT): NULL, OP CODE/REG, WDATA (echo the OP CODE/REG and WDATA values).

SPI READ Sequence

Command sequence (SIN): OP CODE/REG, NULL, NULL.
Response sequence (SOUT): NULL, OP CODE/REG, RDATA (echo the OP CODE/REG and then return the read RDATA value).

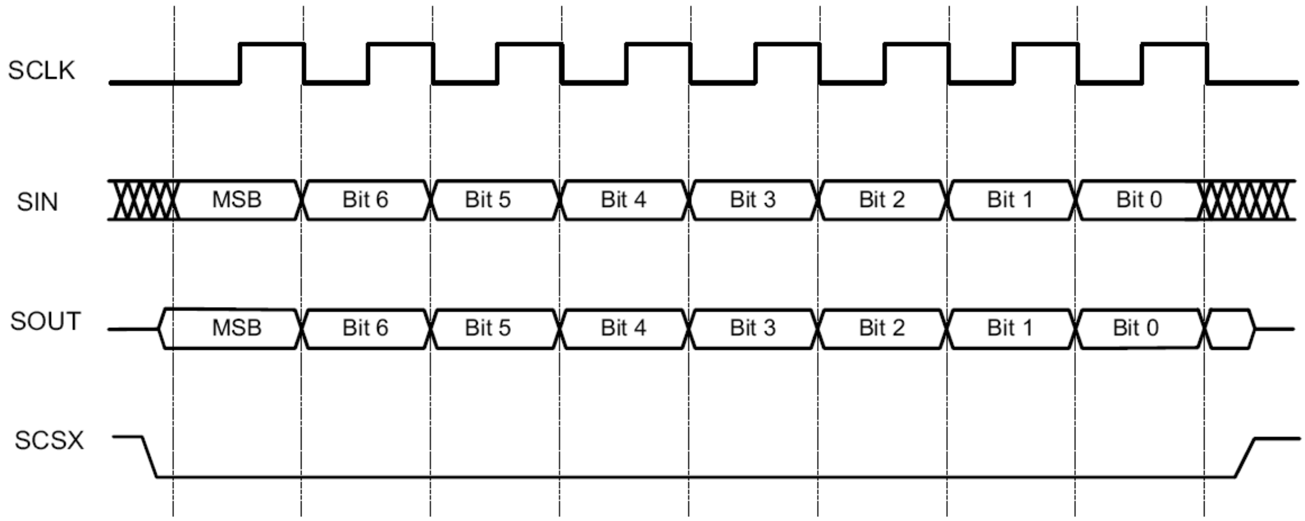
SPI Chip Select

Upon completion of the READ or WRITE operation, the SPI Master must raise the SPI Chip Select (SCSX = 1). For multiple sequential read or write operations, it is required that the SPI Master must raise Chip Select (SCSX = 1) before starting the next SPI transfer. A minimum of 1 SPI clock period is required between sequential SPI operations. The Hybrid Transceiver will ignore all activity on the SCLK and SIN signals when SPI Chip Select is false (SCSX = 1). The SCLK signal may run continuously as in the case of multiple SPI slave devices, but this is not required. The SCLK signal is only sampled by the Hybrid Transceiver when SPI Chip Select is true (SCSX = 0).

SPI Clock

All SIN bits are clocked by the falling edge of SCLK and sampled by the Hybrid Transceiver on the rising edge of SCLK. All SOUT bits are shifted out of the Hybrid Transceiver on the falling edge SCLK and are stable (sampled) on the next falling edge SCLK. Refer to the SPI port detail timing diagram for further clarification. The last bit shifted out on a READ operation is driven on the SOUT line until the SPI Chip Select is driven false (SCSX = 1). After shifting out the last bit (on falling edge clock), all further SCLK cycles are ignored until the SCSX is raised and again lowered to start a new WRITE or READ transaction.

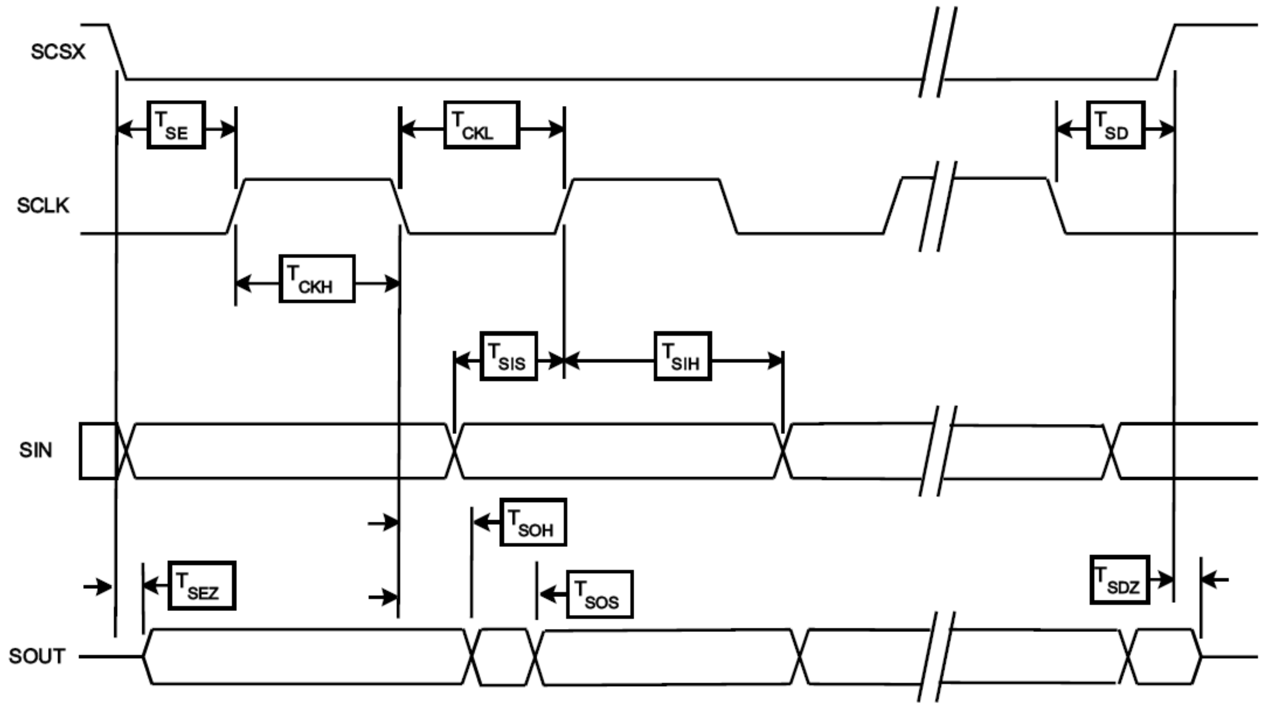
SPI Clock Phase Detail



Notes:

1. SPI Clock (SCLK) shift data on falling edge, sample on rising edge.
2. Single byte transfer shown. Actual transfer requires SCSX to remain low for all 3 bytes.
3. SOUT is driven by the Hybrid Transceiver until the removal of SCSX. See detailed timing diagrams.

SPI Timing Detail

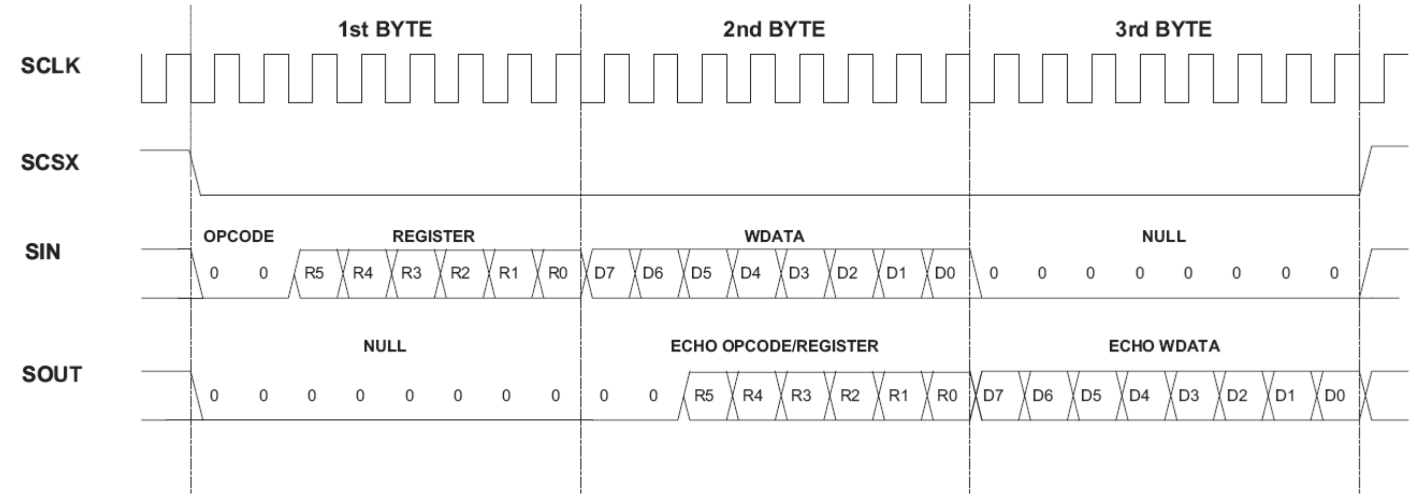


SPI Timing Detail

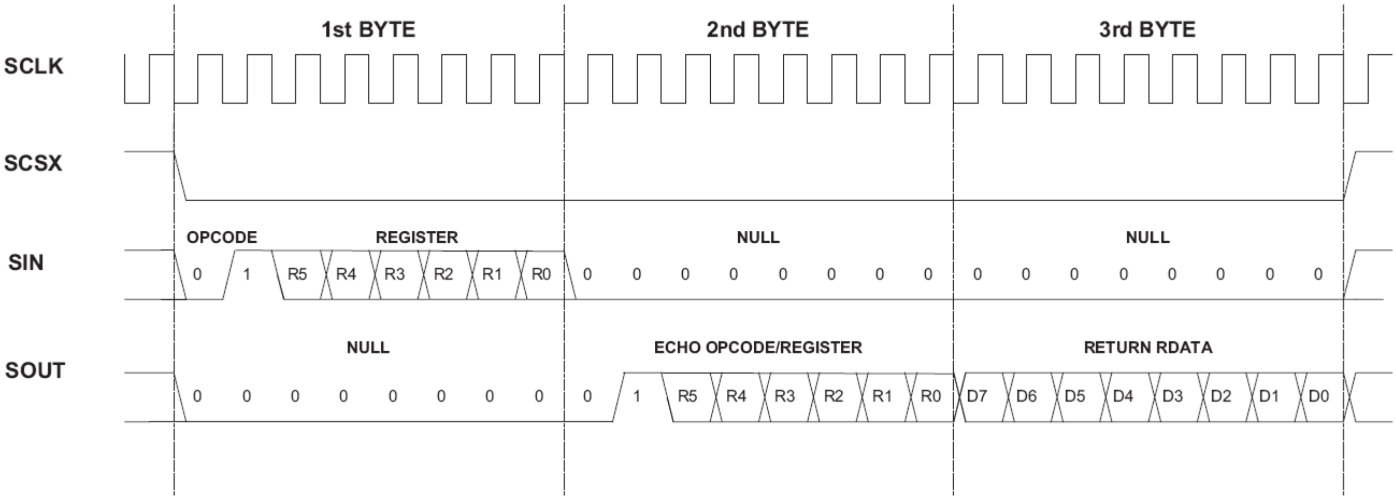
Parameter	Description	MIN	MAX	Unit
SCLK	SPI Transfer rate	0.100	2.0	MHz
T_{SE}	SCSX falling to first edge SCLK	83		ns
T_{SD}	Last SCLK edge to SCSX rising	83		ns
T_{SEZ}	SCSX falling edge to SOUT valid		167	ns
T_{SDZ}	SCSX rising edge to SOUT High-Z		167	ns
T_{CKH}	SCLK High time	208		ns
T_{CKL}	SCLK Low time	208		ns
T_{SIS}	SIN set-up, data valid to SCLK rising edge	83		ns
T_{SIH}	SIN hold, SCLK rising edge to SIN change	83		ns
T_{SOH}	SOUT hold, SCLK falling edge to SOUT change		167	ns
T_{SOS}	SOUT set-up, SCLK falling edge to SOUT valid		292	ns
SCSX High	SCSX High Time between sequential transfers	40		ns

SPI Transfer Sequence Examples

SPI WRITE Operation



SPI READ Operation



Notes:
1. SCLK may run continuously, as in the case of multiple SPI slave devices.
2. SIN Data is sampled on the rising edge SCLK.
3. SOUT Data is shifted on the falling edge of SCLK.
4. All clocks and data outside of SCSX=0 are ignored.
5. The SCSX signal must toggle for at least one SCLK cycle between sequential SPI READ or WRITE operations.

SPI Registers – S/W Control

Register	Symbol	Read/Write	Description
0 through 7	MFG_ID	R	8 byte Manufacturer ID = "STLW FL"
10	PROD_ID	R	Product ID = i.e. 0x01 for HTP-TR4-S001 0x02 for HTP-TR4-S002 0x03 for HTP-TR4-S003, etc.
11	REV_ID	R	Microcode Revision ID
12 13	DATE_CODE1 DATE_CODE0	R	Date Code MSByte, i.e. 0407 = 4th week, 2007 Date Code LSByte
14 15 16 17	USER_ID3 USER_ID2 USER_ID1 USER_ID0	R/W	32 bit storage for User programmable values
20 21 22 23	IDET0 IDET1 IDET2 IDET3	R	RSSI for Channel 0, 1, 2, 3. Signed 8 bit value. Resolution: 1 bit = 0.5dBm Range = -21dBm to -2dBm i.e. -21dBm = 0xD6 and -2dBm = 0xFC
24	TEMPSENS	R	Thermal sense for optical die, Signed 8 bit value. Resolution = 1 bit / °C Range = -50C to +90C
25	RXEN	R/W	RX Channel Enable, 1=Enable, 0=Disable Also requires RXEN H/W pin driven true. Power-up Default = 0x0F b3 = RX Chan 3 Enable b2 = RX Chan 2 Enable b1 = RX Chan 1 Enable b0 = RX Chan 0 Enable
26	RXSD	R	RX Signal Detect, 1=Modulated Optical Signal Present, 0=Not Present b3 = RX Chan 3 SD b2 = RX Chan 2 SD b1 = RX Chan 1 SD b0 = RX Chan 0 SD
34	TXEN	R/W	TX Channel Enable. 1=Enable, 0=Disable Also requires TXEN H/W pin driven true. Power-up Default = 0x0F. b3 = TX Chan 3 Enable b2 = TX Chan 2 Enable b1 = TX Chan 1 Enable b0 = TX Chan 0 Enable

SPI Registers – Continued

Register	Symbol	Read/Write	Description
35	TXSD	R	TX Signal Detect, 1=CML Signal Present, 0=Not Present b3 = TX Chan 3 SD b2 = TX Chan 2 SD b1 = TX Chan 1 SD b0 = TX Chan 0 SD
36	TXFAULT	R	TX Fault Status (1=Fault, 0=No Fault) b7 = Latched TX Fault Chan 3, reset on READ b6 = Latched TX Fault Chan 2, reset on READ b5 = Latched TX Fault Chan 1, reset on READ b4 = Latched TX Fault Chan 0, reset on READ b3 = TX Fault Chan 3 (not latched) b2 = TX Fault Chan 2 (not latched) b1 = TX Fault Chan 1 (not latched) b0 = TX Fault Chan 0 (not latched)
40	SELFTST	R/W	Self Test Control, 1=Initiate, 0=Skip b4 = Self Test complete (1=done, 0=not yet done) b0 through b3 = Any non-zero value initiates self test.
41	SELFSTS	R	Self Test Status, 0x00 = FAIL 0x0F = PASS

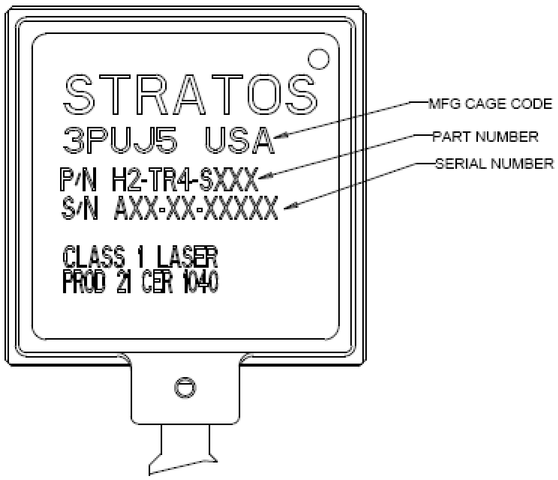
Notes:

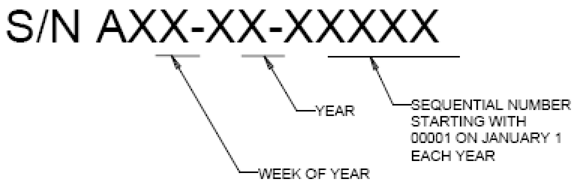
1. All undefined or skipped registers are reserved for future expansion, and SPI writes should not be performed to these locations.
2. The TXEN and RXEN H/W pin can be used to enable/disable all channels via hardware. Individual control of each channel is accomplished via the SPI registers. The H/W pin and SPI register settings are logic ANDed to create the individual channel control.
3. The test requires up to 100msec to complete. At the end of the test, the b4 is set in SELFTST register to indicate test completion and valid status is ready in SELFSTS register. The read-back value for b3-b0 of SELFTST is always a 0.

Ordering Options

Part Number	Name	Description
H2-TR4-SKT-R3	BGA Socket	16x16 BGA surface mount socket, no clip
H2-TR4-CLP-R3	BGA Socket with Clip	16x16 BGA surface mount socket with integrated clip
H2-TR4-S001	Standard Hybrid Transceiver – Option 001	Hybrid Transceiver, 1" fiber length from feedthrough exit, straight fiber route configuration.
H2-TR4-S002	Standard Hybrid Transceiver – Option 002	Hybrid Transceiver, 6" fiber length from feedthrough exit, straight fiber route configuration.
H2-TR4-Sxxx	Hybrid Transceiver	The –Sxxx suffix represents unique part numbering for fiber route and termini options. Consult the factory for details and for custom part numbering for your application.
H2-TR4-PULL	Extraction Tool	Tool to aid in removing the Hybrid Transceiver from the BGA socket.
H2-TR4-PIN	Pin Straightening Tool	Tool to aid in straightening the pins of the Hybrid Transceiver.
H2-TR4-EVAL	HTP EVAL Card	Demonstration and evaluation card, includes support hardware, BGA Socket, and the Hybrid Transceiver.

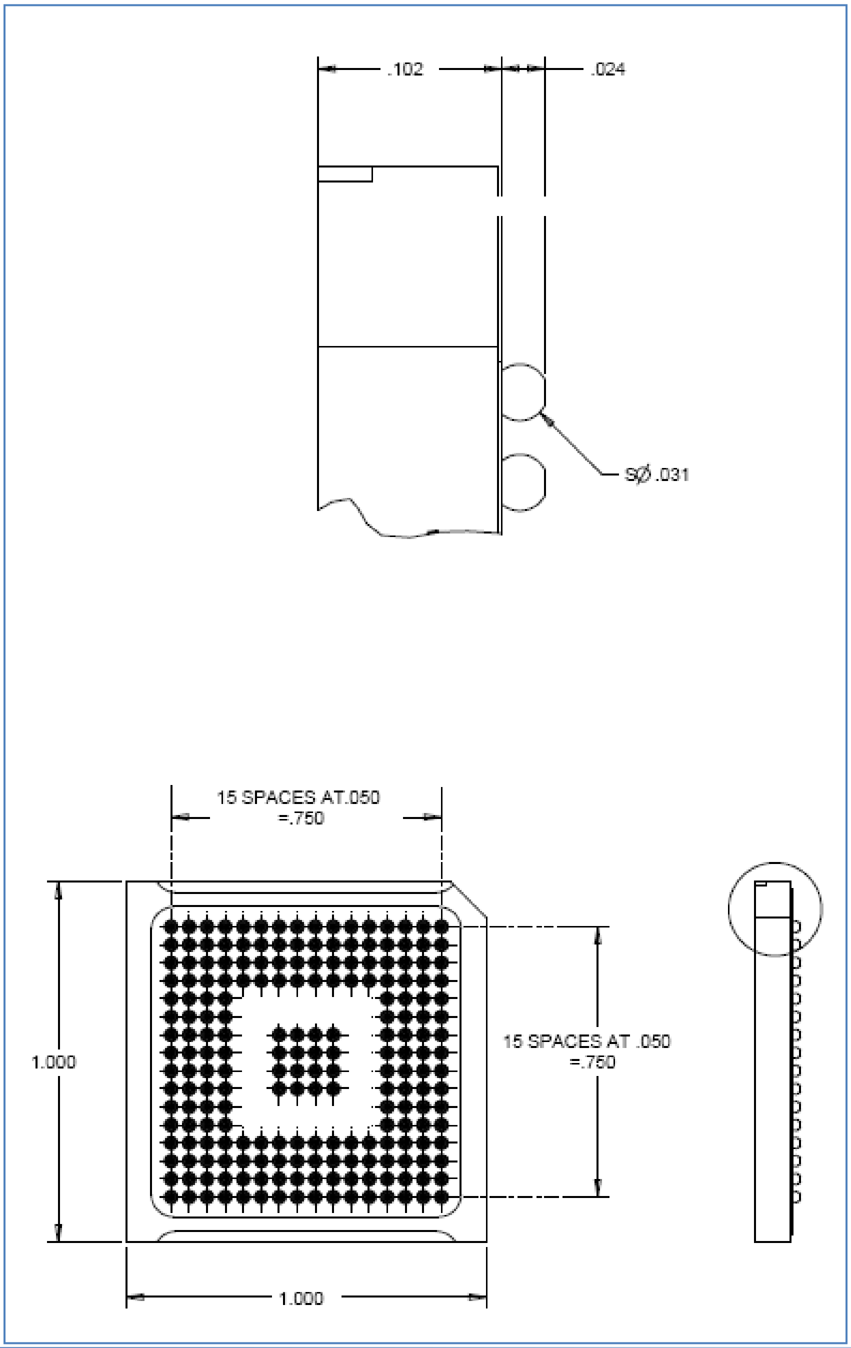
H2-TR4-Sxxx Hybrid Transceiver Label



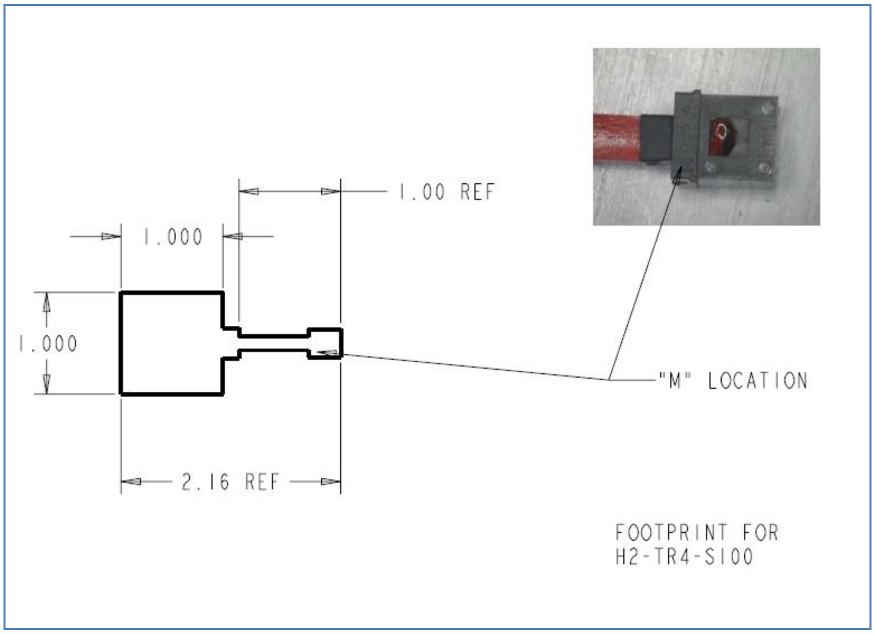


H2-TR4-SKT-R3 Mechanical Detail

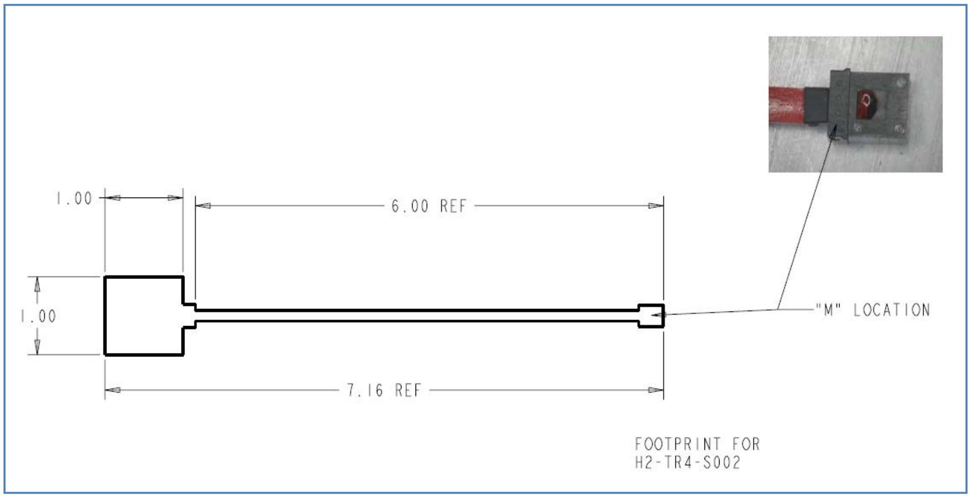
All dimensions are in inches.



Standard H2-TR4-S001 Hybrid Transceiver Footprint



Standard H2-TR4-S002 Hybrid Transceiver Footprint



All dimensions are in inches.

Stratos
H2-TR4-Sxxx
Hybrid Technology Quad Optical Transceiver

Connectivity for Business Critical Continuity

Emerson Connectivity Solutions – Stratos Products
Hybrid Quad Optical Transceiver Worksheet

(Please use this worksheet to specify your order for Hybrid Tranceiver parts)

Customer, Program: ______________________________

____

Data Rate: ______________________________

Fiber Type:

☐ 50/125 µm Graded Index Multimode: Corning OM4 4700 MHz-km Effective Modal Bandwidth

☐ Other: ______________________________

Straight or Shuffle Route:
(If shuffle route then provide Pin# vs Rx,Tx mapping) ______________________________

____

____

Pigtail Length: (+/- 0.5 inches is default)
(If complex routing then provide step file) ______________________________

Special Notes: (Boot color, heatshrink, labels, special testing, shipping, etc.) ______________________________

Part Number: (Assigned by Emerson Connectivity Solutions)	**Assigned By:** (Emerson)	**Date:**

Stratos
H2-TR4-Sxxx
Hybrid Technology Quad Optical Transceiver

Connectivity for Business Critical Continuity

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